MIC & OpenMP 4
TCG Micro
SSG DPD
NERSC Threading Workshop, March 2015
High-performance Parallel Computing

Moving data is expensive!
- Node-node
- Socket-Socket; Processor-(co)processor
- Core-core
- SIMD lanes

At each parallel level
- Find enough parallelism
- Decide the optimal granularity
- Optimize locality/data movement
- Ensure load balance
- Reduce the impact of coordination and synchronization

All the parallel units have to be coordinated with maximum overlap of data movement and computing.
Programming on 61 cores and 244 threads

<table>
<thead>
<tr>
<th></th>
<th>ES-2650 v2 (Ivy Bridge)</th>
<th>Xeon Phi 7120</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Rate GHz</td>
<td>2.40</td>
<td>1.24</td>
</tr>
<tr>
<td># Cores/socket</td>
<td>12</td>
<td>61</td>
</tr>
<tr>
<td># Threads/node (core)</td>
<td>48 (2)</td>
<td>244 (4)</td>
</tr>
<tr>
<td># of sockets</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Peak GFLOP/S</td>
<td>460.8</td>
<td>1210.24</td>
</tr>
</tbody>
</table>

Basics of high-performance parallel computing is much more critical on Xeon™ Phi.

† STREAM bandwidth.
NERSC and community resources

Cori

https://www.nersc.gov/users/computational-systems/cori/

Trainings

https://www.nersc.gov/users/NUG/annual-meetings/nug-2015/hack-a-thon/
https://www.nersc.gov/users/training/events/OMP-vectorization-oct14/

The Intel Xeon Phi User’s Group (IXPUG)

https://www.ixpug.org/what-ixpug
Resources


Intel® Xeon Phi™ Coprocessor

Go Parallel

Get your Intel® Xeon Phi™ coprocessor starter kit today

Productivity via architecture innovation coupled with familiar software. Intel® Xeon Phi™ coprocessor:

GET SUPPORT

Intel® Many Integrated Core Architecture Forum
Parallel Programming Forum
Intel® Premier Support
"I need a cookbook"


http://www.amazon.com/Intel-Xeon-Coprocessor-High-Performance-Programming/dp/0124104142


http://store.elsevier.com/High-Performance-Parallelism-Pearls/James-Reinders/isbn-9780128021187/
OpenMP*: Shared Memory Systems

(Basic) OpenMP How-to:

1. Identify loops with independent operations.
2. Insert compiler directives/pragmas.
3. Add thread synchronization and/or restructure code to avoid data races.
OpenMP*: Shared Memory Systems

Advantages
- Allows incremental development.
- Compiler-driven optimization.
- Support for dynamic load-balancing.

Disadvantages
- Implicit communication ("false sharing").
- Data races are easy to introduce.
- Encourages “bolted on” parallelism.
Intel® Xeon Phi™ Coprocessor: Programming Models

Native

MPI*: Ranks started on device.

OpenMP*: Threads spawned per rank.

SIMD: Vector loops run by threads.

Offload

MPI: Ranks started on host.

OpenMP: Threads spawned in code sections offloaded to device.

SIMD: Vector loops run by threads.

Symmetric

MPI: Ranks started on host/device.

OpenMP: Threads spawned per rank.

SIMD: Vector loops run by threads.
Advanced Offload Use

- Host employs MPI*
- Offload to a part of a device
- Asynchronous computations and communication on the host as usual

Same with host OpenMP* threads

Skipped MPI paths
OpenMP API

- De-facto standard, OpenMP 4.0 out since July 2013
- API for C/C++ and Fortran for shared-memory parallel programming
- Based on directives (pragmas in C/C++)
- Portable across vendors and platforms
- Supports various types of parallelism
Levels of Parallelism in OpenMP 4.0

<table>
<thead>
<tr>
<th>Cluster</th>
<th>Group of computers communicating through fast interconnect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coprocessors/Accelerators</td>
<td>Special compute devices attached to the local node through special interconnect</td>
</tr>
<tr>
<td>Node</td>
<td>Group of processors communicating through shared memory</td>
</tr>
<tr>
<td>Socket</td>
<td>Group of cores communicating through shared cache</td>
</tr>
<tr>
<td>Core</td>
<td>Group of functional units communicating through registers</td>
</tr>
<tr>
<td>Hyper-Threads</td>
<td>Group of thread contexts sharing functional units</td>
</tr>
<tr>
<td>Superscalar</td>
<td>Group of instructions sharing functional units</td>
</tr>
<tr>
<td>Pipeline</td>
<td>Sequence of instructions sharing functional units</td>
</tr>
<tr>
<td>Vector</td>
<td>Single instruction using multiple functional units</td>
</tr>
</tbody>
</table>
NUMA is here to Stay...

- (Almost) all multi-socket compute servers are NUMA systems
  - Different access latencies for different memory locations
  - Different bandwidth observed for different memory locations

- Example: Intel® Xeon E5-2600v2 Series processor
Thread Affinity – Why It Matters?

STREAM Triad, Intel® Xeon E5-2697v2

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Thread Affinity – Processor Binding

- Binding strategies depend on the machine and the app
- Putting threads far, e.g., on different packages
  - (May) improve the aggregated memory bandwidth
  - (May) improve the combined cache size
  - (May) decrease performance of synchronization constructs
- Putting threads close together, e.g., on a core sharing cache
  - (May) improve performance of synchronization constructs
  - (May) decrease the available memory bandwidth and cache size (per thread)
- Affinity is critical to MPI.
Thread Affinity in OpenMP* 4.0

OpenMP 4.0 introduces the concept of places...
- set of threads running on one or more processors
- can be defined by the user
- pre-defined places available:
  - threads: one place per hyper-thread
  - cores: one place exists per physical core
  - sockets: one place per processor package

... and affinity policies...
- spread: spread OpenMP threads evenly among the places
- close: pack OpenMP threads near master thread
- master: collocate OpenMP thread with master thread

... and means to control these settings
- Environment variables OMP_PLACES and OMP_PROC_BIND
- clause proc_bind for parallel regions
Thread Affinity Example

Example (Intel® Xeon Phi™ Coprocessor): Distribute outer region, keep inner regions close

```
OMP_PLACES=cores(8); OMP_NUM_THREADS=4,4; OMP_PROC_BIND=spread,close
```

Alternatively,

```
#pragma omp parallel proc_bind(spread)
#pragma omp parallel proc_bind(close)
```
Vectorization: SIMD Machines

OpenMP* 4.0 SIMD How-to:

1. Identify loops with independent operations.
2. Insert compiler directives/pragmas.
3. Follow compiler’s recommendations to enable/improve generated vector code.
Vectorization: SIMD Machines

Advantages

- Allows incremental development.
- Compiler-driven optimization.
- Lanes are always synchronized.

Disadvantages

- Data structure/alignment requirements.
- Knowledge of ISA required to ensure efficient scalar to vector conversion.
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